



Bias Resistor Transistors

NPN Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

FEATURES

- Reduces board space
- Simplifies Circuit Design
- Reduces Board Space and Component Count
- Qualified to AEC-Q101 Standards for High Reliability

Mechanical Data

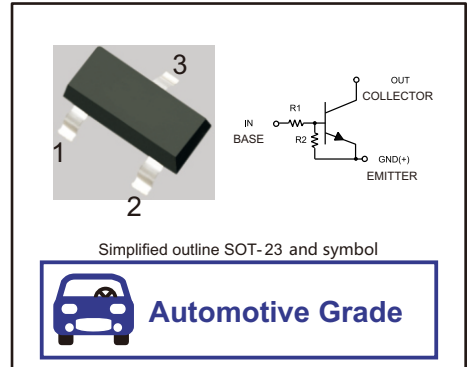
- Case: SOT-23
- $R_1 = 4.7K\Omega$ (Typ) , $R_2 = 4.7K\Omega$ (Typ)

MAXIMUM RATINGS (Ta =25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	V
Collector-Emitter Voltage	V_{CEO}	50	V
Output current	I_C	100	mA
Power dissipation	P_D	200	mW
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	625	°C/W
Junction temperature	T_J	150	°C
Range of storage temperature	T_{stg}	-55~ +150	°C

PINNING

PIN	DESCRIPTION
1	BASE
2	EMITTER
3	COLLECTOR



ELECTRICAL CHARACTERISTICS (TA = 25°C unless otherwise noted.)

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Collector-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\mu A, I_E = 0$	50			V
Collector-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 2mA, I_B = 0$	50			V
Emitter-base breakdown voltage	$V_{(BR)EBO}$	$I_E = 2mA, I_C = 0$	10			V
Collector-Base Cut off Current	I_{CBO}	$V_{CB} = 50V, I_E = 0$			100	nA
Collector-Emitter Cut off Current	I_{CEO}	$V_{CE} = 50V, I_B = 0$			0.5	uA
Emitter-Base Cut off Current	I_{EBO}	$V_{EB} = 6V, I_C = 0$			1.5	mA
DC Current Gain	h_{FE}	$V_{CE} = 10V, I_C = 5mA$	15	30		
Output Voltage (on)	V_{OL}	$V_{CE} = 5.0V, V_{BE} = 2.5V, R_L = 1.0K \Omega$			0.2	V
Output Voltage (off)	V_{OH}	$V_{CE} = 5.0V, V_{BE} = 0.5V, R_L = 1.0K \Omega$	4.9			V
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 10mA, I_B = 1mA$			0.25	V
Input Voltage(off)	$V_{I(off)}$	$V_{CE} = 5V, I_C = 100\mu A$	0.5			V
Input Voltage(on)	$V_{I(on)}$	$V_{CE} = 0.3V, I_C = 20mA$			3	V
Input resistance	R_1		3.3	4.7	6.1	K Ω
Input resistance	R_2		3.3	4.7	6.1	K Ω
Resistance ratio	R_2 / R_1		0.8	1.0	1.2	



Typical Performance Characteristics

Fig 1. VCE(sat) versus IC

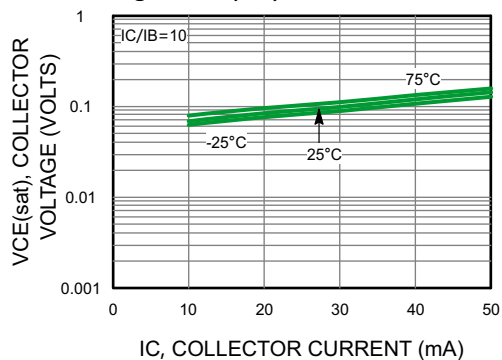


Fig 2. DC Current Gain

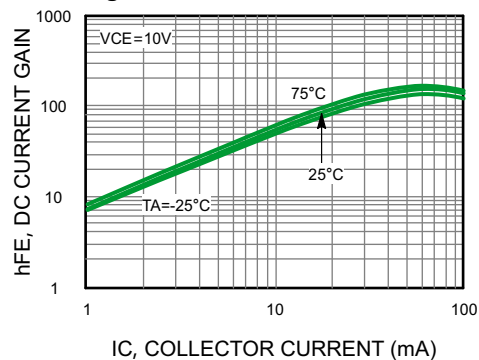


Fig 3. Output Capacitance

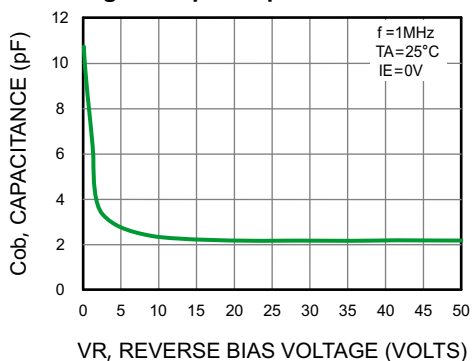


Fig 4. Output Current versus Input Voltage

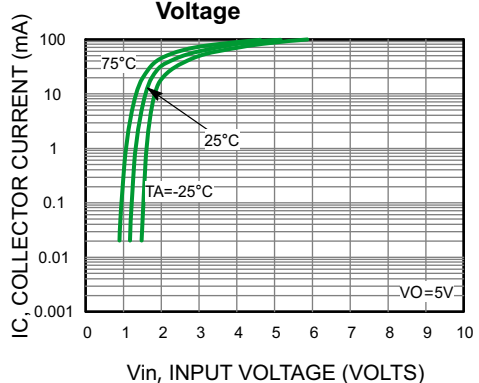
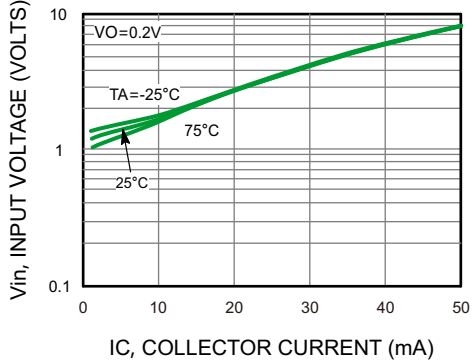
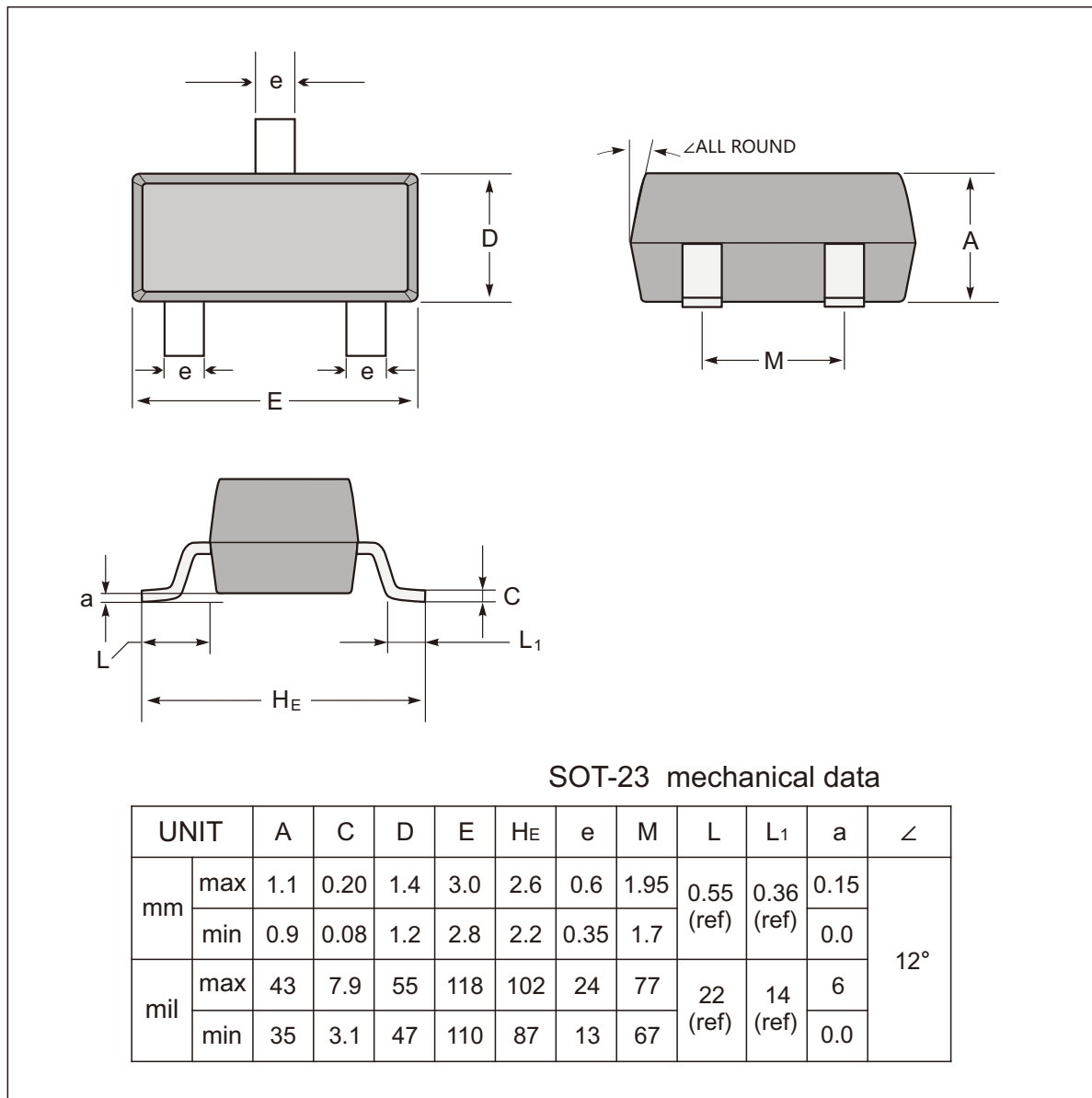


Fig 5. Input Voltage versus Output Current

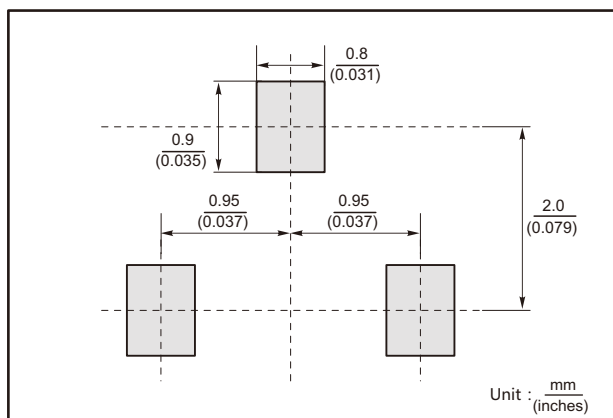




SOT-23 Package Outline Dimensions



The recommended mounting pad size



Marking

Type number	Marking code
JDTC143EWD	43E



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